CLAIMS

What is Claimed is:

1. A multiply-MAC (multiply accumulate) circuit comprising:

a first register operative to store a first data, wherein said first register is addressable using a first address which disables an accumulate operation and is addressable using a second address which enables a MAC operation; and

a second register operative to store a second data, wherein said second register is addressable using a third address which disables said accumulate operation and is addressable using a fourth address which enables said MAC operation.

2. A multiply-MAC circuit as recited in Claim 2 further comprising:

a multiplier circuit coupled to said first and second registers, wherein said multiplier circuit is operative to perform a multiply operation to generate a product value based on data in said first and second registers after a write operation is performed on any one of said first and second registers; and

an accumulator circuit coupled to said multiplier circuit, wherein said accumulator circuit is operative to perform said accumulate operation to generate an accumulate value based on said product value and a previous accumulate value if any one of said second and fourth addresses is used in said write operation.

3. A multiply-MAC circuit as recited in Claim 2 wherein if any one of said first and third addresses is used in said write operation, said previous accumulate value is not changed.

4. A multiply-MAC circuit as recited in Claim 1 wherein said first address is a primary address and wherein said second address is an alias address.

5. A multiply-MAC circuit as recited in Claim 1 wherein said third address is a primary address and wherein said fourth address is an alias address.

6. A circuit for selectively performing a multiply operation and a MAC (multiply accumulate) operation, comprising:

a first register operative to store a first data, wherein said first register is addressable using a first address which indicates said multiply operation is selected and is addressable using a second address which indicates said MAC operation is selected;

a second register operative to store a second data, wherein said second register is addressable using a third address which indicates said multiply operation is selected and is addressable using a fourth address which indicates said MAC operation is selected;

a multiplier circuit coupled to said first and second registers, wherein said multiplier circuit is operative to perform said multiply operation to generate a product

value based on data in said first and second registers after a write operation is performed on any one of said first and second registers; and

an accumulator circuit coupled to said multiplier circuit, wherein said accumulator circuit is operative to perform an accumulate operation to generate an accumulate value based on said product value and a previous accumulate value if any one of said second and fourth addresses is used in said write operation.

7. A circuit as recited in Claim 6 wherein said first address is a primary address and wherein said second address is an alias address.

8. A circuit as recited in Claim 6 wherein said third address is a primary address and wherein said fourth address is an alias address.

9. A circuit as recited in Claim 6 wherein if any one of said first and third addresses is used in said write operation, said previous accumulate value is not changed.

10. A circuit as recited in Claim 6 wherein after a first MAC operation is performed and before a second MAC operation is performed, a first multiply operation is performed without changing a first accumulate value associated with said first MAC operation.

11. A controller comprising:

a first register operative to store a first data, wherein said first register is addressable using a first address which indicates a multiply operation is selected and is addressable using a second address which indicates a MAC (multiply accumulate) operation is selected;

a second register operative to store a second data, wherein said second register is addressable using a third address which indicates said multiply operation is selected and is addressable using a fourth address which indicates said MAC operation is selected;

a multiplier circuit coupled to said first and second registers, wherein said multiplier circuit is operative to perform said multiply operation to generate a product value based on data in said first and second registers after a write operation is performed on any one of said first and second registers; and

an accumulator circuit coupled to said multiplier circuit, wherein said accumulator circuit is operative to perform an accumulate operation to generate an accumulate value based on said product value and a previous accumulate value if any one of said second and fourth addresses is used in said write operation.

12. A controller as recited in Claim 11 wherein said first address is a primary address and wherein said second address is an alias address.

13. A controller as recited in Claim 11 wherein said third address is a primary address and wherein said fourth address is an alias address.

14. A controller as recited in Claim 11 wherein if any one of said first and third addresses is used in said write operation, said previous accumulate value is not changed.

15. A controller as recited in Claim 11 wherein after a first MAC operation is performed and before a second MAC operation is performed, a first multiply operation is performed without changing a first accumulate value associated with said first MAC operation.

16. A controller comprising:

a first register operative to store a first data, wherein said first register is addressable using a first address which disables an accumulate operation and is addressable using a second address which enables said accumulate operation; and

a second register operative to store a second data, wherein said second register is addressable using a third address which disables said accumulate operation and is addressable using a fourth address which enables said accumulate operation.

17. A controller as recited in Claim 16 further comprising:

a multiplier circuit coupled to said first and second registers, wherein said multiplier circuit is operative to perform a multiply operation to generate a product value based on data in said first and second registers after a write operation is performed on any one of said first and second registers; and

an accumulator circuit coupled to said multiplier circuit, wherein said accumulator circuit is operative to perform said accumulate operation to generate an accumulate value based on said product value and a previous accumulate value if any one of said second and fourth addresses is used in said write operation.

18. A controller as recited in Claim 17 wherein if any one of said first and third addresses is used in said write operation, said previous accumulate value is not changed.

19. A controller as recited in Claim 16 wherein said first address is a primary address and wherein said second address is an alias address.

20. A controller as recited in Claim 16 wherein said third address is a primary address and wherein said fourth address is an alias address.

21. A method of selectively performing a multiply operation and a MAC (multiply accumulate) operation, comprising the steps of:

a) writing a data to a register using one of a first address which indicates said multiply operation is selected and a second address which indicates said MAC operation is selected;

b) performing said multiply operation to generate a product value based on said data; and

c) performing an accumulate operation to generate an accumulate value based on said product value and a previous accumulate value if said second address is used in said step a).

22. A method as recited in Claim 21 wherein said first address is a primary address and wherein said second address is an alias address.

23. A method as recited in Claim 21 wherein if said first address is used in said step a), said previous accumulate value is not changed.